

FIG. 1

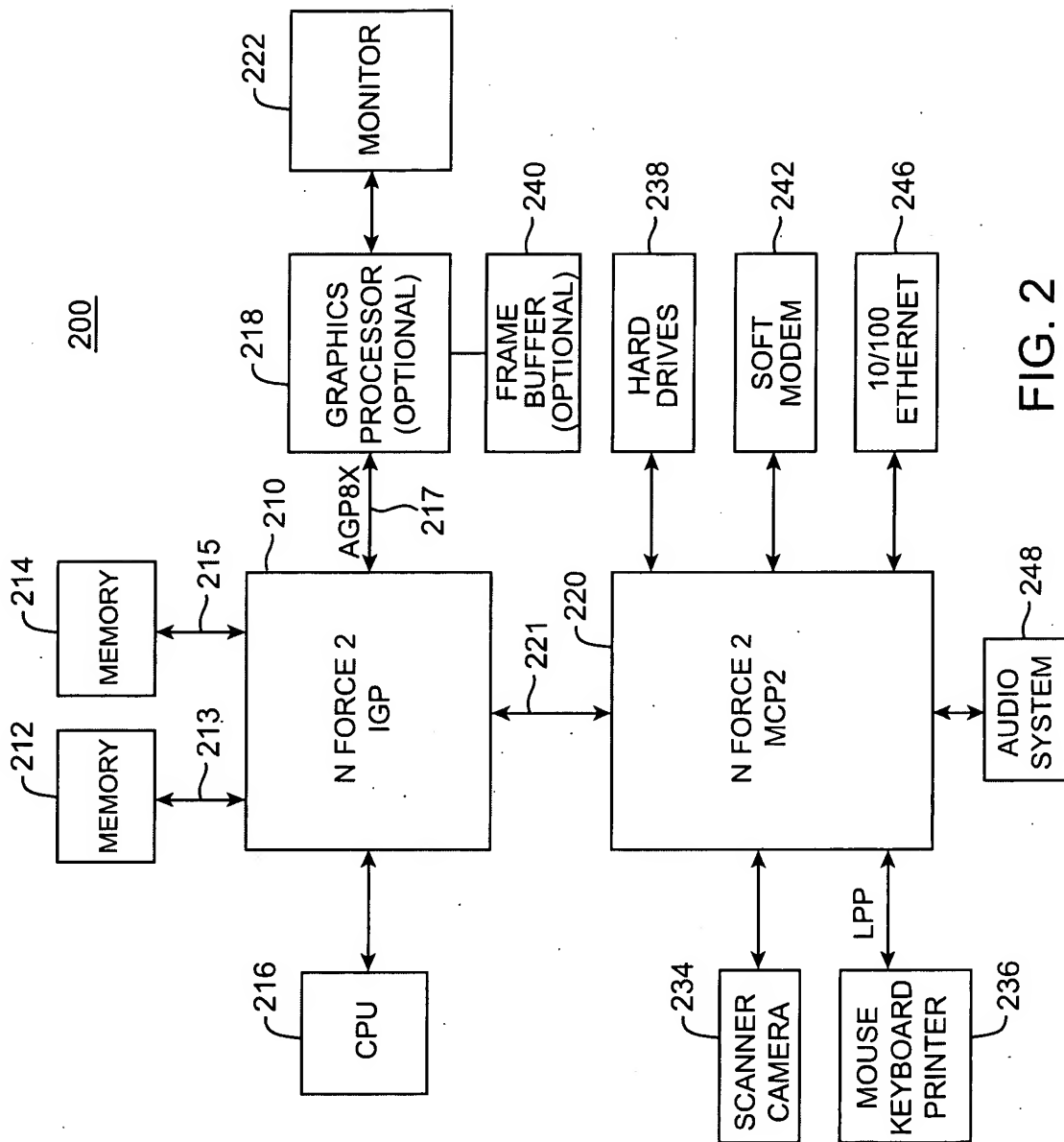
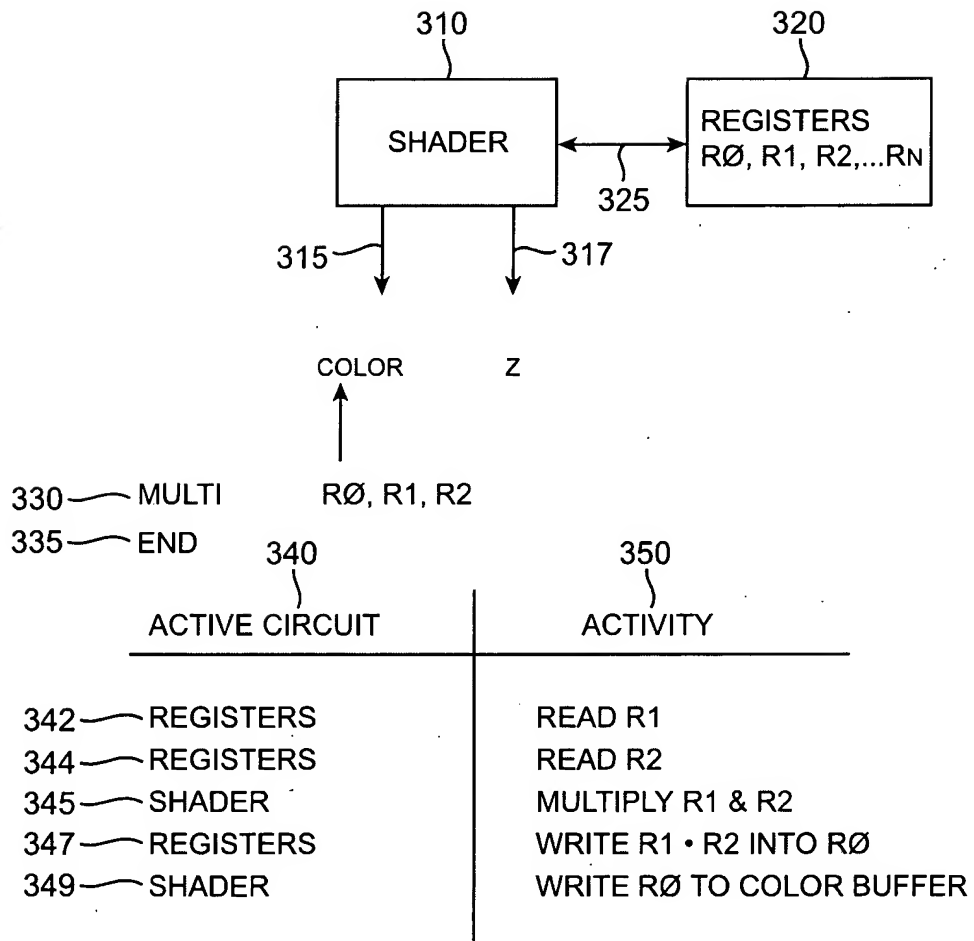
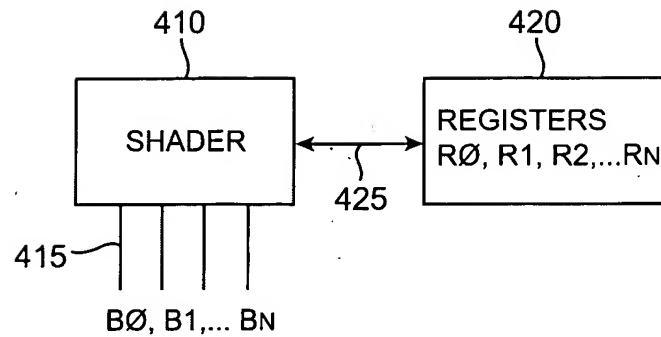


FIG. 2



PRIOR ART
FIG. 3



430 — MULTI R0, R1, R2
 440 — ADD R1, R0, R1
 450 — END

MORE BUFFERS =
 MORE STEPS PER PASS +
 FEWER PASSES

460 ACTIVE CIRCUIT	470 ACTIVITY
462 — REGISTERS	READ R1
464 — REGISTERS	READ R2
466 — SHADER	MULTIPLY R1 & R2
468 — REGISTERS	WRITE R1 • R2 INTO R0
472 — REGISTERS	READ R0
474 — REGISTERS	READ R1
476 — SHADER	ADD R0 & R1
478 — REGISTERS	WRITE R0 + R1 INTO R1
482 — SHADER	WRITE R0 AND R1 INTO BUFFERS

FIG. 4

510 — MULTI RØ, R1, R2

520 — PST RØ, #ZL

530 — ADD RØ, R3, R4

540 — PLD R1, #ZH

550 — PLD RØ, #id INDIRECT (FIXED)

552 — PLD RØ, @ R1 IDENTIFICATION (MOVABLE)

554 — PLD RØ, # address DIRECT REFERENCE

556 — PLD RØ, @ R1 ADDRESS

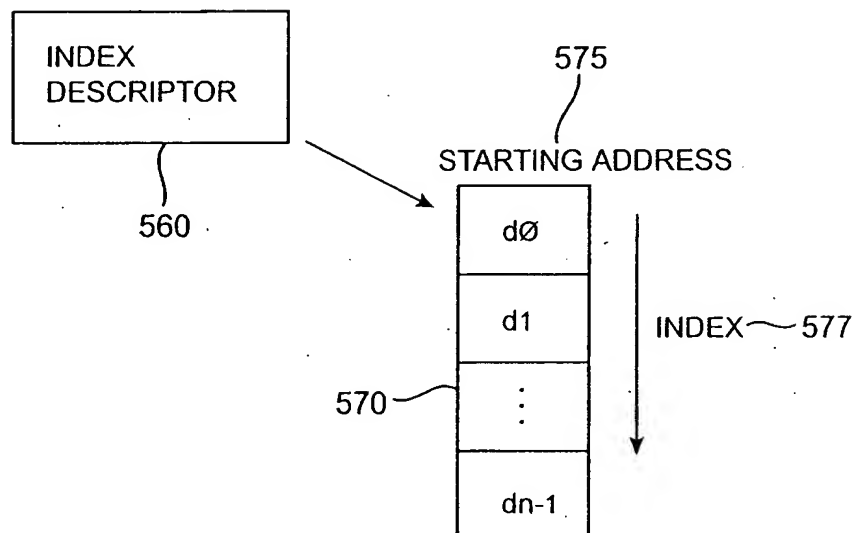


FIG. 5

610 — IF ($Z_L < Z$ AND $Z < Z_H$) SET $Z_H = Z$

620 — IF ($Z \leq Z_L$) SET $Z_H = Z_L$, SET $Z_L = Z$

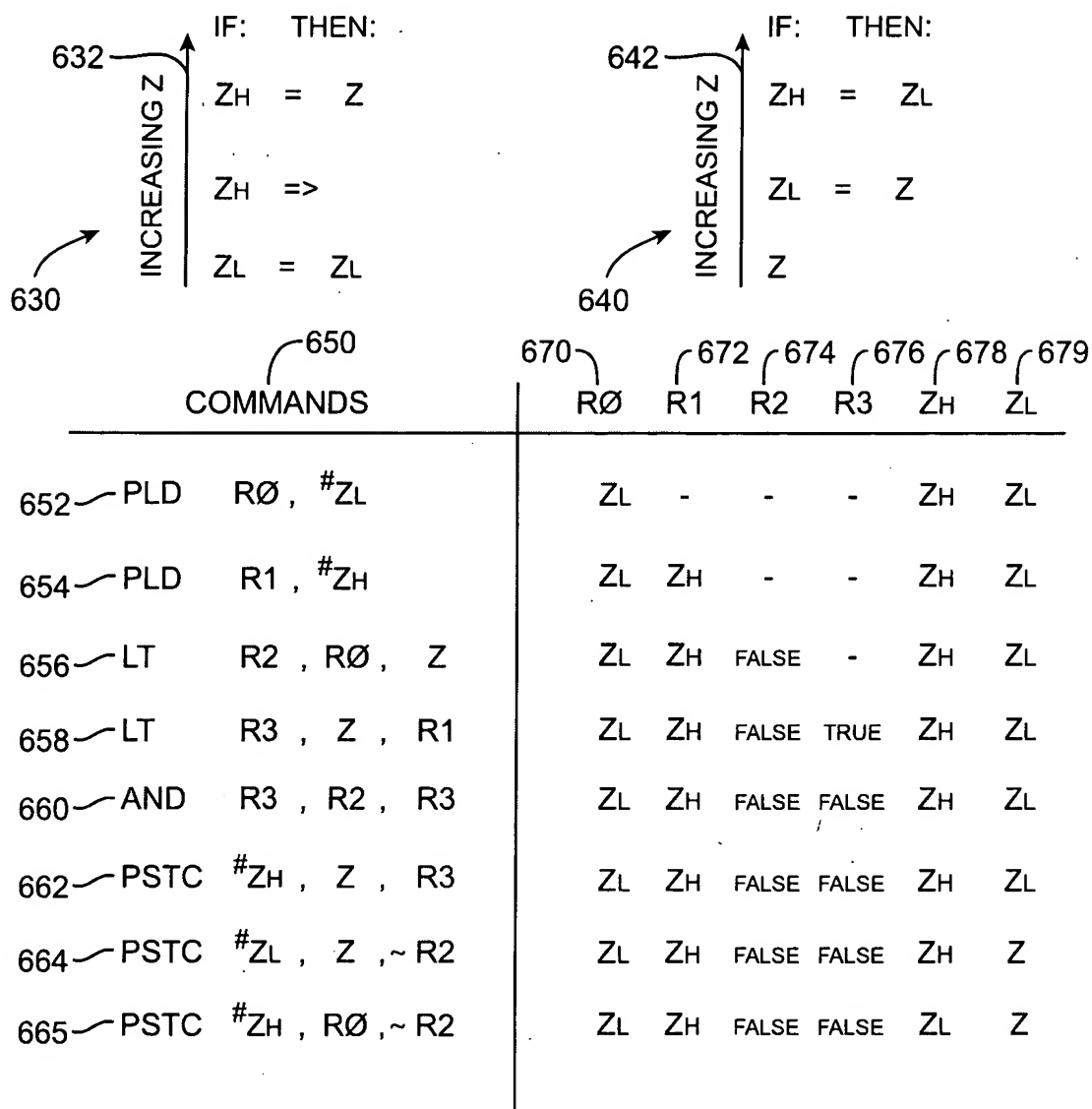


FIG. 6

